WHAT IS CLAIMED IS:

1. A radio communication apparatus in a CDMA communication system which has a plurality of delay profile circuits for generating delay profiles by calculating correlations between a reception signal and known data at a plurality of timings, and timing circuits which are respectively prepared for said delay profile circuits and generate correlation timings in said delay profile circuits,

wherein operation of at least one of said delay profile circuit which generated the delay profile and said timing circuit for generating a correlation timing in said delay profile circuit is stopped in accordance with a correlation value of the delay profile.

2. An apparatus according to claim 1, wherein said plurality of delay profile circuits are used to simultaneously receive signals from a plurality of CDMA transmitters, and operation of at least one of said delay profile circuit which generated the delay profile and said timing circuit for generating a correlation timing in said delay profile circuit is stopped in accordance with a correlation value of the delay profile during handover operation of switching from one of said plurality of CDMA transmitters to another CDMA transmitter.

3. An apparatus according to claim 1, wherein when a

largest correlation value of the delay profile is smaller than a predetermined threshold, operation of at least one of said delay profile circuit which generated the delay profile and said timing circuit for generating a correlation timing in said delay profile circuit is stopped.

4. An apparatus according to claim 2, wherein when a largest correlation value of the delay profile is smaller than a predetermined threshold, operation of at least one of said delay profile circuit which generated the delay profile and said timing circuit for generating a correlation timing in said delay profile circuit is stopped.

5. An apparatus according to claim 1, wherein when the number of delay profile circuits is represented by N (N is a natural number satisfying $2 < N$), and largest correlation values of delay profiles respectively generated by said plurality of delay profile circuits are represented by Pb(N), Pb(N-1),..., Pb(1) in decreasing order of values, operation of at least one of said delay profile circuit which generated a delay profile exhibiting a largest correlation value Pb(i) and said timing circuit for generating a correlation timing in said delay profile circuit is stopped if (Pb(N) - Pb(i)) (i is a natural number satisfying $1 \leqq i < N$) is larger than a

predetermined threshold.

6. An apparatus according to claim 2, wherein when the number of delay profile circuits is represented by N (N is a natural number satisfying 2 < N), and largest correlation values of delay profiles respectively generated by said plurality of delay profile circuits are represented by Pb(N), Pb(N-1),..., Pb(1) in decreasing order of values, operation of at least one of said delay profile circuit which generated a delay profile exhibiting a largest correlation value Pb(i) and said timing circuit for generating a correlation timing in said delay profile circuit is stopped if (Pb(N) - Pb(i)) (i is a natural number satisfying $1 \leqq i < N$) is larger than a predetermined threshold.

7. An apparatus according to claim 1, wherein when the number of delay profile circuits is represented by N (N is a natural number satisfying 2 < N), and largest correlation values of delay profiles respectively generated by said plurality of delay profile circuits are represented by Pb(N), Pb(N-1),..., Pb(1) in decreasing order of values, operation of at least one of said delay profile circuit which generated a delay profile exhibiting a largest correlation value Pb(i-1) ~ (Pb(1) and said timing circuit for generating a correlation timing in said delay profile circuit is stopped if (Pb(N) - Pb(i)) (i is

a natural number satisfying $1 \leqq i < N$) is larger than a predetermined threshold.

8. An apparatus according to claim 2, wherein when the number of delay profile circuits is represented by N (N is a natural number satisfying $2 < N$), and largest correlation values of delay profiles respectively generated by said plurality of delay profile circuits are represented by Pb(N), Pb(N-1),..., Pb(1) in decreasing order of values, operation of at least one of said delay profile circuit which generated a delay profile exhibiting a largest correlation value Pb(i-1) ~ (Pb(1) and said timing circuit for generating a correlation timing in said delay profile circuit is stopped if (Pb(N) - Pb(i)) (i is a natural number satisfying $1 \leqq i < N$) is larger than a predetermined threshold.

9. An apparatus according to claim 1, wherein a predetermined period of time during which operation of said delay profile circuit is stopped is a natural number multiple of a length of a radio frame of a reception signal.

10. An apparatus according to claim 2, wherein a predetermined period of time during which operation of said delay profile circuit is stopped is a natural number multiple of a length of a radio frame of a reception signal.

11. An apparatus according to claim 1, wherein operation of at least one of said delay profile circuit and said timing circuit is stopped by stopping supplying an operation clock to at least one of said delay profile circuit and said timing circuit.

12. An apparatus according to claim 2, wherein operation of at least one of said delay profile circuit and said timing circuit is stopped by stopping supplying an operation clock to at least one of said delay profile circuit and said timing circuit.

13. An apparatus according to claim 1, wherein operation of at least one of said delay profile circuit and said timing circuit is stopped by stopping supplying power to at least one of said delay profile circuit and said timing circuit.

14. An apparatus according to claim 2, wherein operation of at least one of said delay profile circuit and said timing circuit is stopped by stopping supplying power to at least one of said delay profile circuit and said timing circuit.

15. A radio communication apparatus used in a CDMA communication system, comprising an antenna for receiving signals from base stations, a radio circuit for performing quadrature detection and modulation with respect to the signals received through said antenna, a plurality of

delay profile circuits for obtaining delay profiles by calculating correlations between the signals from said radio circuit and known data, a searcher circuit for selecting a delay profile exhibiting a large correlation value from the plurality of delay profiles obtained by said delay profile circuits, and outputting a signal on which a despreading timing is based, a plurality of timing circuits for outputting pulse signals representing correlation timings in said delay profile circuits on the basis of the signal from said searcher circuit, a CPU for controlling operations of said delay profile circuits and said timing circuits, and an operation clock generating circuit for generating and outputting operation clocks for operating said delay profile circuits and said timing circuits,

wherein when a largest correlation value of the delay profile is smaller than a predetermined threshold, a stop request signal for stopping operation of said delay profile circuit that generated the delay profile is output from said searcher circuit to said CPU, and

said CPU performs control to stop operation of at least one of said delay profile circuit and said timing circuit corresponding thereto upon receiving the stop request signal.

16. An apparatus according to claim 15, wherein when

a predetermined period of time has elapsed after said searcher circuit outputs the stop request signal, said searcher circuit stops outputting the stop request signal.

17. An apparatus according to claim 15, wherein operation of at least one of said delay profile circuit and said timing circuit is stopped by stopping supplying an operation clock to at least one of said delay profile circuit and said timing circuit.

18. An apparatus according to claim 15, wherein operation of at least one of said delay profile circuit and said timing circuit is stopped by stopping supplying power to at least one of said delay profile circuit and said timing circuit.

19. A power consumption control method for a radio communication apparatus which is used in a CDMA communication system and has a plurality of delay profile circuits for generating delay profiles by calculating correlations between a reception signal and known data at a plurality of timings, comprising:

the comparison step of comparing a largest correlation value of the delay profile with a predetermined threshold; and

the stop step of stopping operation of said delay profile circuit on the basis of the comparison result obtained in the comparison step.

20. A method according to claim 19, wherein the stop step comprises stopping operation of said delay profile circuit when the largest correlation value is smaller than the predetermined threshold.

21. A method according to claim 19, further comprising:

the step of detecting whether a predetermined period of time elapses while operation of said delay profile circuit is stopped in the stop step; and

the step of resuming the operation of said delay profile circuit when a lapse of the predetermined period of time is detected in the detection step.

22. A power consumption control method for a radio communication apparatus which is used in a CDMA communication system and has a plurality of delay profile circuits for generating delay profiles by calculating correlations between a reception signal and known data at a plurality of timings and timing circuits prepared for the respective delay profile circuits to generate correlation timings therein, comprising:

the comparison step of comparing a largest correlation value of the delay profile with a predetermined threshold; and

the stop step of stopping operation of said delay profile circuit on the basis of the comparison result

obtained in the comparison step.

23. A power consumption control method for a radio communication apparatus which is used in a CDMA communication system and has a plurality of delay profile circuits for generating delay profiles by calculating correlations between a reception signal and known data at a plurality of timings and timing circuits prepared for the respective delay profile circuits to generate correlation timings therein, comprising:

the comparison step of comparing a largest correlation value of the delay profile with a predetermined threshold;

the first stop step of stopping operation of said delay profile circuit on the basis of the comparison result obtained in the comparison step; and

the second stop step of stopping operation of said timing circuit on the basis of the comparison result obtained in the comparison step.